Trade Space Involved with Single Event Upset (SEU) and Transient (SET) Handling of Field Programmable Gate Array (FPGA) Based Systems

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Outline

- **FPGA Background**
  - **Space Usage**
  - **Technologies**

- **Trading the parameter space**
  - **Constraints for FPGA usage**
  - **Prioritizing the constraints**
  - **SEUs and SETs**
  - **Optimization?**

- **Example trade**

- **Summary**

Faulty Chips Delay Launch of Japanese Imaging Satellite

PAUL KALLENDER-UMEZU, TOKYO
MISSY FREDERICK, WASHINGTON

The Japanese government has decided to postpone the launch of the nation's next reconnaissance satellite by six months or more following the discovery of potentially defective integrate-circuits in the satellite, a government official said August 26.

The Prime Minister's Cabinet Office, which is in charge of the nation's Information Gathering Satellite (IGS) program, decided Aug. 25 to postpone the launch of what would be the nation's third reconnaissance satellite in orbit after deciding it was necessary to replace a number of field programmable gate array (FPGA) chips made by Actel Corp. of Mountain View, Calif., according

to Yasuhiro Itakura, research officer at Japan's Cabinet Satellite Intelligence Center, which is part of the Cabinet Office.

The satellite, which carries an optical sensor, was to have been launched by a Japanese H-2A rocket from the Tanegashima Launch Center before the end of March 2006, but it will take about six months to replace the potentially faulty chips and test the satellite to prepare it for flight, Itakura said in an August 26 telephone interview.

Some 10 chips need to replaced, he said. Details about when the problem was discovered were not available at the time of the interview.

Problems with Actel's earlier version of its FPGA were discovered in autumn 2003, after more than 1 million of the devices were

shipped to various vendors.

Ken O'Neill, director of military and aerospace product marketing for Actel, said after news of the defect became known, Actel supplied the Japanese government with the latest version of the company's FPGA, which the company has the option to install in place of the old version. Since then, the government has been doing reliability testing of both the old and new product, though Actel had not received official word that the company would be replacing the chips as of press time, O'Neill said.

Actel believes the new version of the FPGA should not cause any further problems, O'Neill said.

"They have been tested pretty extensively, and clearly show a very high level of reliability," O'Neill said. "We have confidence that the

reliability of the earlier version is high, but the latest version of the software does offer a higher level of reliability," he said.

FPGAs contain hundreds of thousands of programmable elements, according to O'Neill, and the defect found in the old version of the chips affected one antifuse within the design, causing it to fail. O'Neill said the chips that do fail usually do so early in the lifetime of the part.

As a supplier, Actel is not directly involved with the rebuilding process, O'Neill said.

The other scheduled flight of a radar-type satellite, which is due for launch sometime in the Japanese government's 2006 fiscal year (April 2006-March 2007), is not affected by the problem with the Actel chips, and its launch schedule has not been al-

tered, Itakura said.

Each of the the next information-gathering satellites to be launched will have the same capabilities as the original satellites launched by an H-2A rocket in March 2003. One type of satellite has an optical sensor capable of 1-meter resolution, while the radar-type satellite has a resolution of 1-3 meters.

The IGS program was developed in response to an August 1998 incident when North Korea launched a missile that overflew Japanese territory and landed in the Pacific. Two more satellites were slated to join the first pair in orbit in November 2003, but those satellites were destroyed when the H-2A rocket carrying them failed.

Comments: mfrederick@space.com

Space News article on FPGA Issue on a satellite

What is an FPGA?

- **A Field Programmable Gate Array (FPGA) is a building block electronic device that consists of:**
  - **An array of logic modules,**
  - **An input/output ring, and**
  - **A programmable interconnect.**
  - ***All on a CMOS silicon base.***
- **An FPGA may replace everything from simple logic to complex processors to ASIC devices in a space system.**
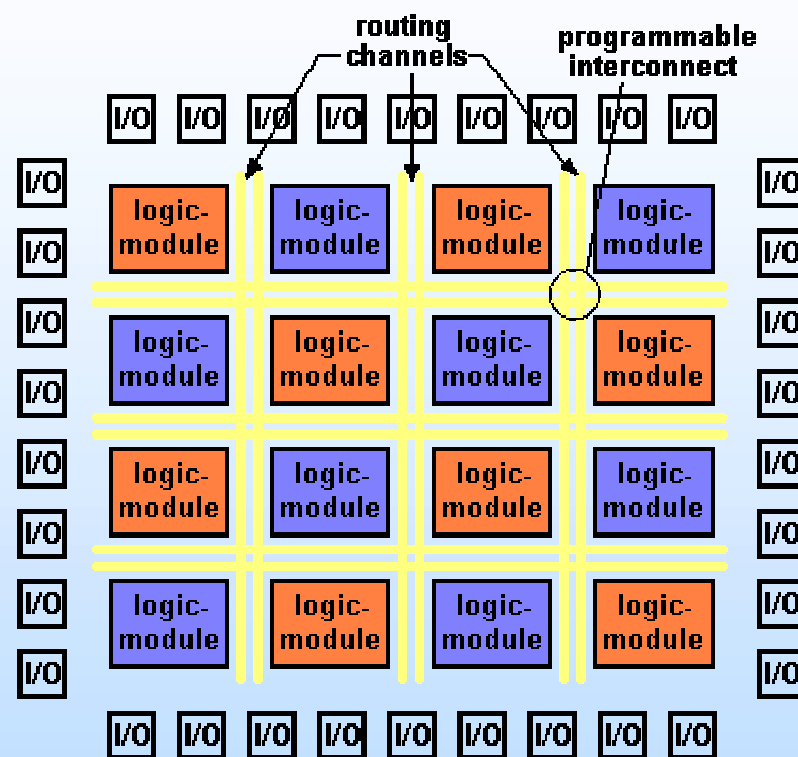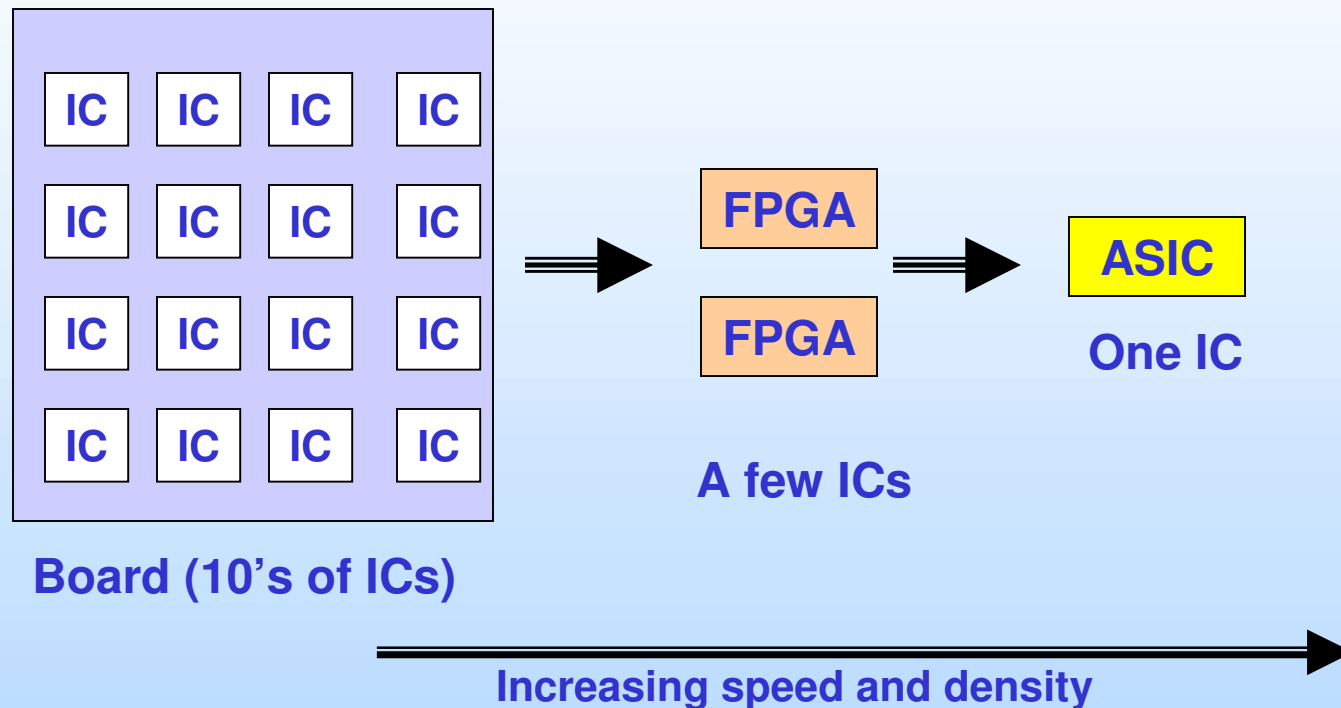

FPGA-architecture

Using FPGAs in a System

- **Before FPGAs, electronic systems comprised of standard standalone off-the-shelf devices and/or custom-designed application specific integrated circuits (ASICs). In essence,**
  - **Standard devices are convenient for availability, but do not provide an optimal solution (power, size) for a specific problem, while,**
  - **ASICs provide a high-performance solution, but at a cost and schedule risk.**
- **FPGAs combine many of the features of both types of devices, providing reasonably high-performance while being an off-the-shelf device.**
  - **Recent FPGAs may also include dedicated silicon structures in addition to the programmable interconnect called hard *intellectual property* or hard IP. This increases device performance in that the overhead associated with the routing/interconnect technologies are minimized.**
  - ***Soft IP* is simply having "pre-compiled" drop-in functions that utilize Logic Blocks in the device via design software tools.**

Near-ASIC performance plus off-the-shelf availability = FPGAs

Where FPGAs Fit in a Electrical System/Integrated Circuit (IC) Hierarchy

IC	IC	IC	IC
IC	IC	IC	IC
IC	IC	IC	IC
IC	IC	IC	IC

FPGA

FPGA

ASIC

One IC

A few ICs

Board (10's of ICs)
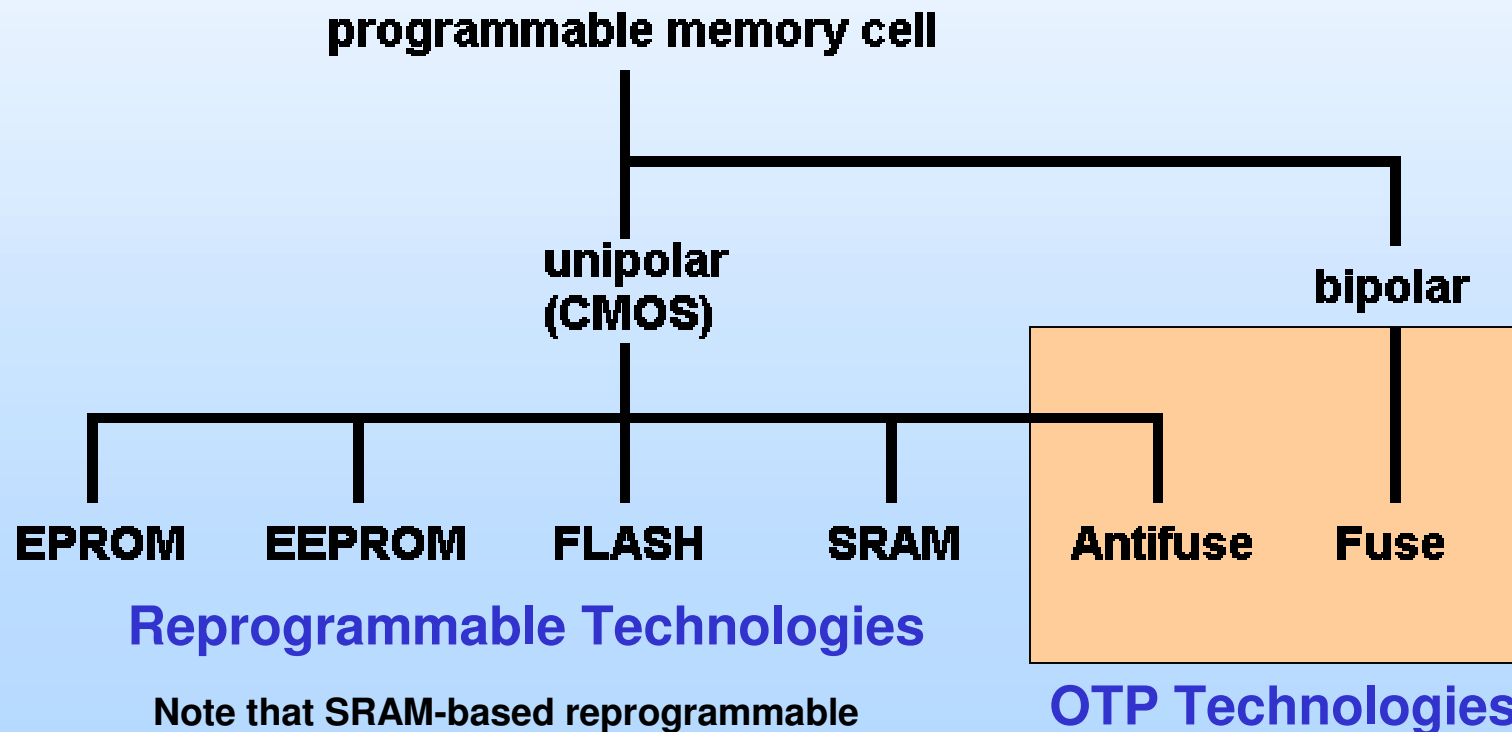
Increasing speed and density

FPGA Technologies

- **Different manufacturers have used different approaches to the interconnect fabric.**

- **A quick method of discriminating FPGA types can be broken into one-time programmable (OTP) and reprogrammable devices.**

- **OTP devices are much like a traditional Programmable Read Only Memory (PROM) in that they traditionally have their interconnect structure "burned" in by an external piece of equipment and this configuration (how the logic and I/O is connected) is non-volatile and not subject to being changed.**

- **Reprogrammable devices typically do not require such a piece of equipment (except EPROM technology devices) and their configuration may or may not be non-volatile depending on the technology that FPGA is implemented with for configuring the device.**
  - **Non-volatile for these devices implies that configuration storage takes place on the FPGA of interest and does not need to be stored externally.**
  - **Conversely, volatile devices require an external storage element prior to loading it into the device for usage.**

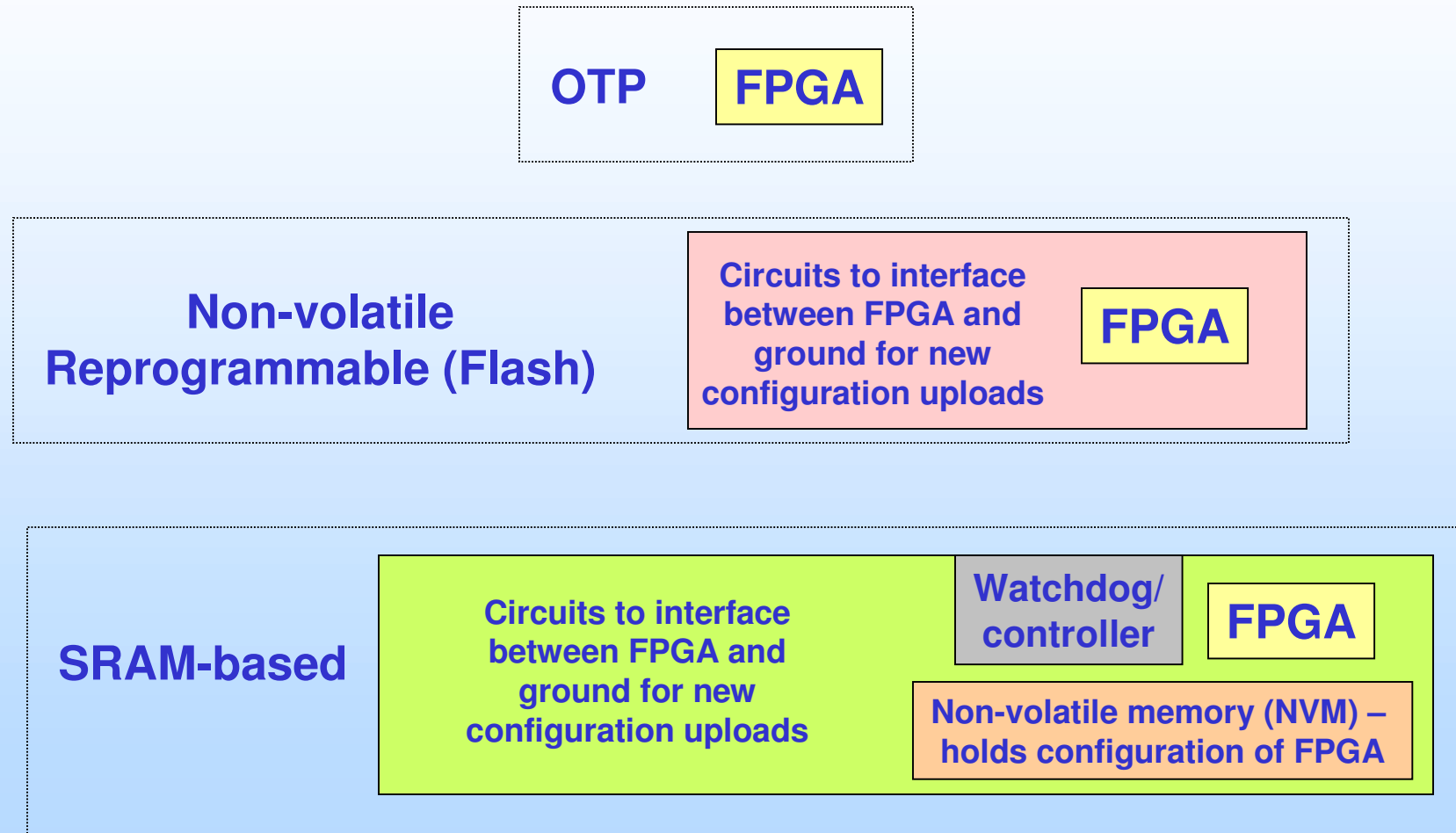# Example FPGA Configuration Technologies

- **The method of configuration and configuration storage of a device is critical in understanding the differences in FPGA technologies**
  - **Each FPGA implementation technique has it's pros and cons and should be chosen based on specific system needs for performance, reliability, radiation tolerance, etc…**

programmable memory cell

unipolar (CMOS)   **bipolar**

EPROM   **EEPROM**   **FLASH**   **SRAM**   **Antifuse**   **Fuse**

Reprogrammable Technologies

Note that SRAM-based reprogrammable devices are sometimes called latch-based

OTP Technologies

Sample System Complexity by Technology Types

OTP   **FPGA**

Non-volatile Reprogrammable (Flash)

Circuits to interface between FPGA and ground for new configuration uploads   **FPGA**

SRAM-based

Circuits to interface between FPGA and ground for new configuration uploads   **Watchdog/ controller**   **FPGA**

Non-volatile memory (NVM) – holds configuration of FPGA

FPGAs for Space Systems

- **There are currently five known vendors that market devices specifically to the space market.**
- **They are**
  - **Actel (antifuse OTP)**
  - **Aeroflex (antifuse OTP)**
  - **Xilinx (reprogrammable latch-based)**
  - **ATMEL (reprogrammable SRAM-based), and,**
  - **Honeywell (reprogrammable SRAM-based).**
- **It should be noted that the Honeywell device is the only traditional radiation-hardened product of the group, but suffers from two flaws:**
  - **Small number of gates (a metric used for electrical designs), and,**
  - **Is available ONLY as a board-level product making it impractical to be integrated into many systems.**
- **The prime US aerospace market share for FPGAs is dominated by Actel and Xilinx, but Aeroflex (new rad-hard offering) and ATMEL (rad-tolerant) are relatively new to market.**
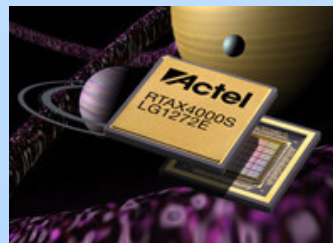
Comparing the "Big Three"

- **Aeroflex – "The Toyota"**
  - **Moderate performance**
  - **Designed for reliability and radiation hardness**
    - *Needs more testing*
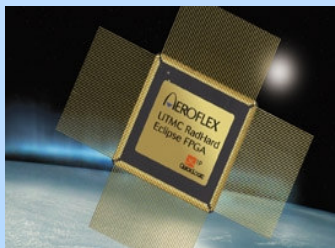
- **Actel – "The Infiniti"**
  - **Good performance**
  - **Reliable and fairly radiation tolerant**
    - *EXPENSIVE to fix when broken*

- **Xilinx – "The Jaguar"**
  - **Indy-car performance**
  - **Designed for commercial usage; requires a personal mechanic to keep running in space!**
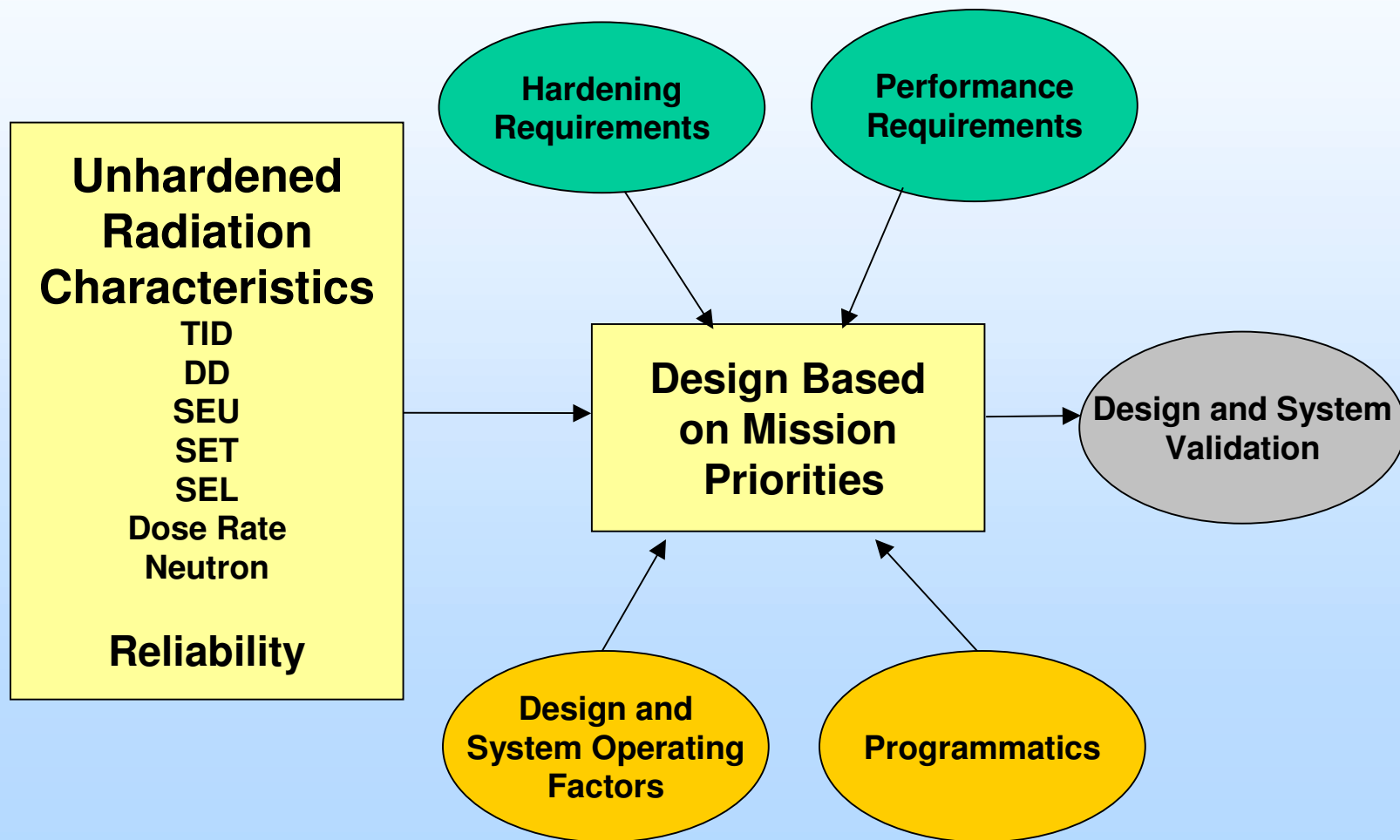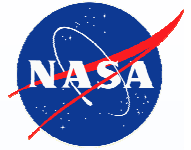
The Trade Space –
Considerations for Device Selection (Sample List)

- **Cost**
  - Procurement
  - NRE
  - Maintenance
  - Qualification and test
- **Schedule**
- **System performance factors**
  - Speed
  - Power
  - Volume
  - Weight
  - System function and criticality
  - Other mission constraints (example, reconfigurability)
- **System Complexity**
  - Secondary ICs (and all their associated challenges)
  - Software, etc…

- **Design Environment and Tools**
  - Existing infrastructure and heritage
- **Simulation tools**
- **System operating factors**
  - Operate-through for single events
  - Survival-through for portions of the natural environment
  - Data operation (example, 95% data coverage)
- **Radiation and Reliability**
  - SEE rates
  - Lifetime (TID, thermal, reliability,…)
  - "Upscreening"
- **System Validation and Verification**

Note:
The last two are often the most ignored!

Simplifying the View –
A Radiation Person's Perspective

Unhardened Radiation Characteristics
- TID
- DD
- SEU
- SET
- SEL
- Dose Rate
- Neutron

Reliability

Hardening Requirements

Performance Requirements

Design Based on Mission Priorities

Design and System Validation

Design and System Operating Factors

Programmatics

Mission Priorities Drive System Choices

- **Given the same function, not every space mission will consider the SAME constraints as their priority. In other words,**

  - **Mission A may need data processing real-time and have speed of performance as their first priority,**

  - **Mission B may need to gather science during solar events and have radiation as their first priority,**

  - **Mission C may have a long lifetime and be focused on reliability and radiation lifetime, while**

  - **Mission D may be weight constrained.**

- **Typically, the program has been given specific priorities, some of which are in conflict with each other.**
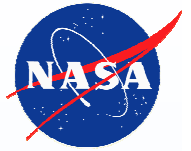
Comparison of Aeroflex and Xilinx Devices – Sample Candidates for a Trade Space

Feature	Aeroflex	Xilinx
Family	Eclipse	Virtex-IV
Process	0.25um CMOS/epi	90nm CMOS (copper)
Technology	OTP	Reprogrammable (latch)
Sample Hard IP cores	RAM	RAM, dual PowerPC 405, DSP slices, Ethernet, Rocket I/O (to 10 GHz)
Datapath speed	150 MHz	>500 MHz
Logic	>300K usable gates*	>200K logic cells*
TID	300 krads-SI guaranteed	Commercial, expect >100 krads-Si
SEU	Moderate	Upsets with protons
SEL	Immune	???

*** "Marketing" gates and cells – realistically Virtex-IV is >> bigger than the Eclipse**

FPGA Trade Space presented by Kenneth LaBel, HEART Conference, Santa Clara, CA, March 7, 2006

The Crux Of This Presentation –
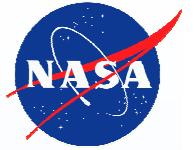# Radiation with Emphasis on SEUs and SETs Versus Mission Priorities

- **Given that mission priorities vary, dealing with the SEU/SET question and system implementation vary as well.**

- **Some systems solutions may best be met with a simpler system implementation that may be less "powerful", but can more easily meet schedule constraints, while,**

- **Some systems prefer higher performance that require a much more complex system design AND validation (but will drive to a longer development cycle)**
  - **Using the Xilinx Virtex family as a sample, we will look at the types of SEUs/SETs that can occur in such a complex architecture**

Representative Xilinx Virtex Family-
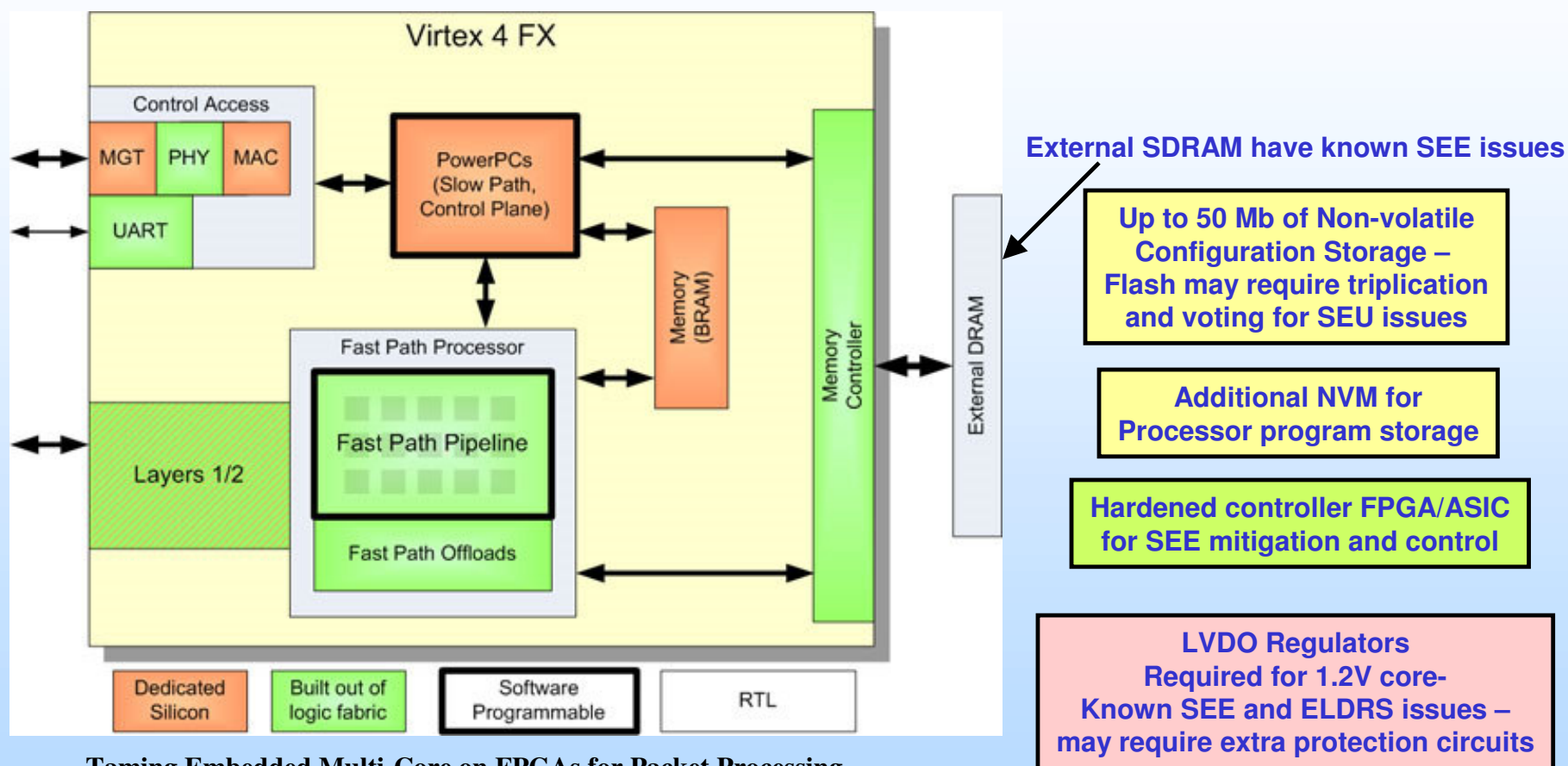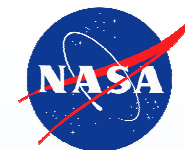# Potential Types of Device SEE Sensitivity
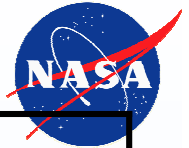
Chip Area	SEE Issue	Possible SEU Mitigation
Config. Memory	Single and multiple bit errors corrupting circuit operation, causing bus conflicts (current creep), etc…	• Scrubbing • Partial reconfiguration
Config. Controller	Improper device configuration can occur if hit during configuration/reconfiguration	• Partitioned design • Multiple chip voting (Redundancy by using multiple devices)
CLB	Logic hits and propagated upsets caused by transients	• Triple modular redundancy (TMR) (or Xilinx TMR – XTMR) • Acceptable error rates
BRAM	Memory upsets in user area	• TMR • Error Detection and Correction (EDAC) scrubbing
Half-latches	Sensitive structure used in configuration/routing	• Removal of half-latches from design
POR	SEUs on POR can cause inadvertent reboot of device	Multiple chip voting (Redundancy by using multiple devices)
IOB	SEUs can cause false outputs to other devices or inputs to logic	• Leverage Immune Config. Memory cell • Evaluate input SET propagation
DCM	Can cause clock errors that spread across clock cycles	• TMR • Temporal TMR
DSP	Hard IP that is unhardened that can cause single event functional interrupts (SEFIs) or data errors	• TMR • Temporal TMR
MGT	Gigabit transceivers. Hits in logic can cause bursts or SEFIs. O/w bit errors in data stream	• TMR • Protocol re-writes
PPC	Hard IP that is unhardened. SEFIs are prime concern	• TMR or software task redundancy
SEL	Higher current condition that is potentially damaging	• No mitigation other than substrate addition (epi). • Circumvention techniques possible

May Not Need to Mitigate ALL Types of Events

Example Mission Application Requirements

- **Embedded image controller**
  - **Packet processing application**
  - **Real-time jitter control**
  - **Long-duration object staring**
  - **Image recognition and target tracking**
- **The big question in this type of application comes down to:**
  - **Do you need to ensure that you track every single target or do you have time for a "hiccup" now and then?**
    - **Science may be able to take a hiccup**
    - **Weapons arena may not**
  - **Drives systems operability requirements**

Sample Implementing Architecture Using Xilinx Virtex-IV FX Device

External SDRAM have known SEE issues

Up to 50 Mb of Non-volatile Configuration Storage – Flash may require triplication and voting for SEU issues

Additional NVM for Processor program storage

Hardened controller FPGA/ASIC for SEE mitigation and control

LVDO Regulators Required for 1.2V core- Known SEE and ELDRS issues – may require extra protection circuits

Taming Embedded Multi-Core on FPGAs for Packet Processing
by Bryon Moyer, Teja Technologies, Inc
http://www.fpgajournal.com/articles_2006/20060131_teja.htm

Higher reliability may drive triplicate device option w/voting

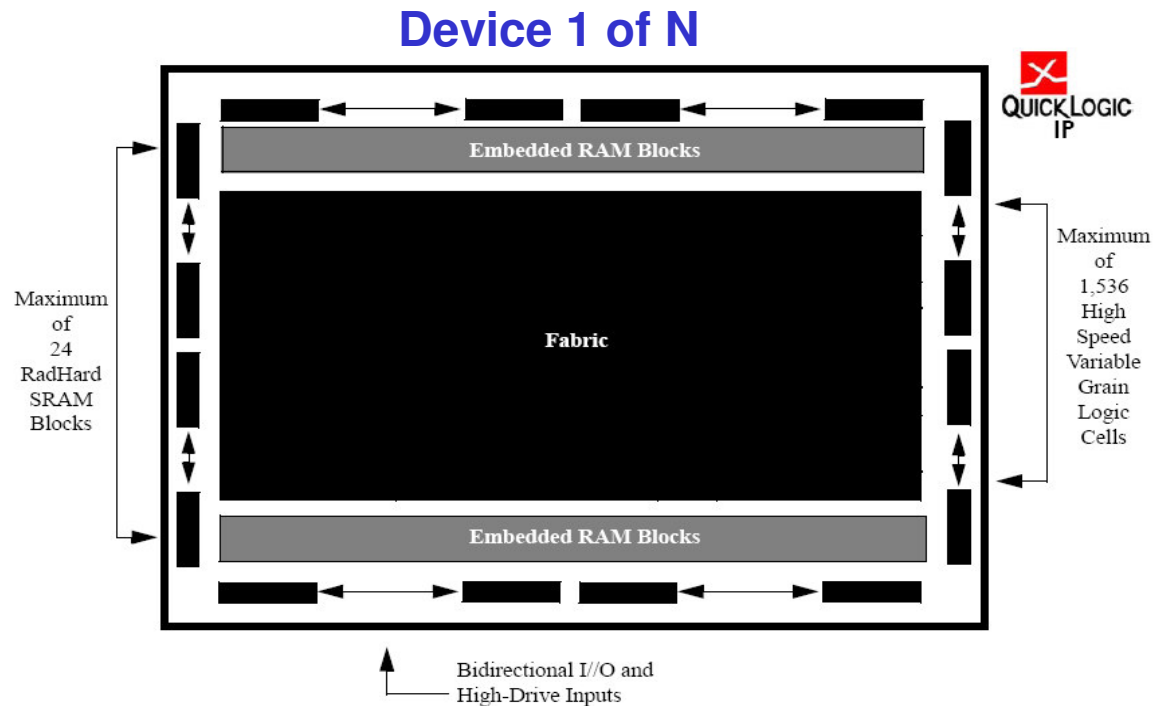# Sample Implementing Architecture Using Aeroflex Eclipse Device

Device 1 of N

Figure 1. RadHard Eclipse FPGA Block Diagram

2.5V and 3.3V Regulators Available Rad Hard

Processing functions done w/soft IP

http://ams.aeroflex.com/ProductFiles/DataSheets/FPGA/RadHardEclipseFPGA.pdf

Architectural Impact within The Xilinx Design Flow

- **Scrubbing Mitigation:**
  - An additional Hardened FPGA is required (ACTEL or Aeroflex) to implement the scrubbing control.
  - Extra Flash Memory is required (with voting and correction ability) that will store configuration
- **XTMR Mitigation**
  - Triple the I/O and the design (impact power, Area, and board complexity)
  - Inserted after synthesis (irregular design flow can complicate system validation)
- **Advantage:**
  - Large device can implement System On a Chip and reduce complexity of general design
  - Speed

Architectural Impact within The Aeroflex Design Flow

- **Aeroflex – The necessity of additional FPGAs is the largest impact:**
  - **Extra logic for FPGA to FPGA interface communication/Synchronization is necessary**
    - **Interface control document!**
  - **Can complicate Board Design**
  - **Requires careful Architectural decision making concerning the partitioning scheme**
  - **Speed can be affected**
- **Advantage**
  - **SEU/SET tolerance is built into the silicon and will not require extra mitigation at this level of the system implementation**
  - **System Level Validation and Implementation is generally less complicated**

Design Methodology Flowcharts:
Aeroflex vs. Xilinx

Aeroflex: Partioning Concerns

Additional Partitioning Logic, Board Layout, Possible Speed/Performance Hit, Synchronization →

Additional Architectural Design Considerations:

VHDL (Functionality Creation)

Synthesis (Gate Level Creation)

Place and Route

Blow Corresponding Antifuses

Same Design Flow Path as a Commercial Product

Xilinx: Mitigation Concerns

Additional Architectural Design Considerations:

← Additional FPGA for Scrubbing, Additional Memory for Scrubbing, Board Layout (triple I/O), Possible Speed/Performance Hit

VHDL (Functionality Creation)

Synthesis (Gate Level Creation)

Same Design Flow Path as a Commercial Product

Insert XTMR

Place and Route

Program Device

Same Design Flow Path as a Commercial Product

Verification Flow: Aeroflex vs. Xilinx

Aeroflex

VHDL

Synthesis

Gate Level

Test Bench/Simulator
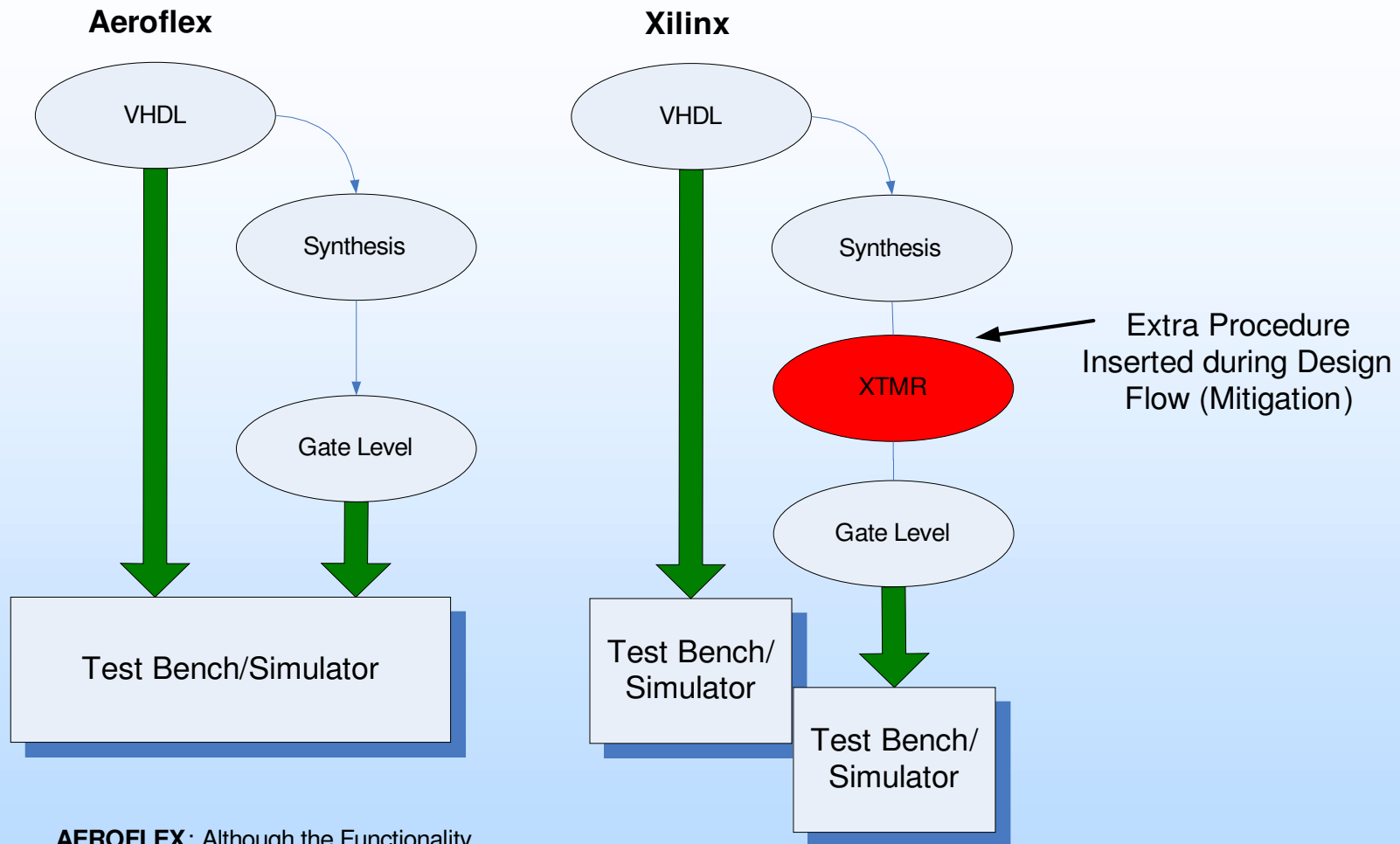
**AEROFLEX**: Although the Functionality has been Partitioned, the same test bench can be used at the VHDL level and at the Gate Level

Xilinx

VHDL

Synthesis

XTMR ← Extra Procedure Inserted during Design Flow (Mitigation)

Gate Level
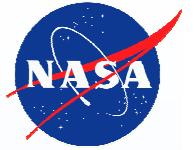
Test Bench/Simulator

Test Bench/Simulator

Xilinx: Due to the triple I/O (and extra mitigation logic), The user may need to implement 2 separate test benches – Pure Black box testing will not require a large difference in each Test Bench

System Validation and Fault Tolerance Considerations

- **General Considerations**
  - **Failure Rate Prediction and Quantification (if possible)**
  - **Recovery Time upon Failure/Data Loss**
  - **Difficulty of Recovery (I.e. Reboot, Power Down, etc…)**
  - **Difficulty of System Validation after mitigation insertion**
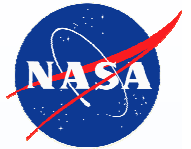 - **Is it easier to have four designers working with one chip or four?**
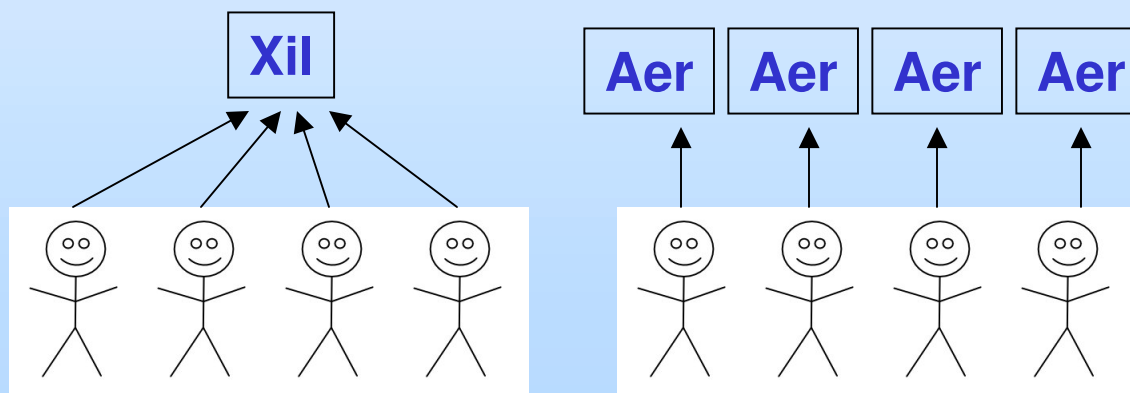
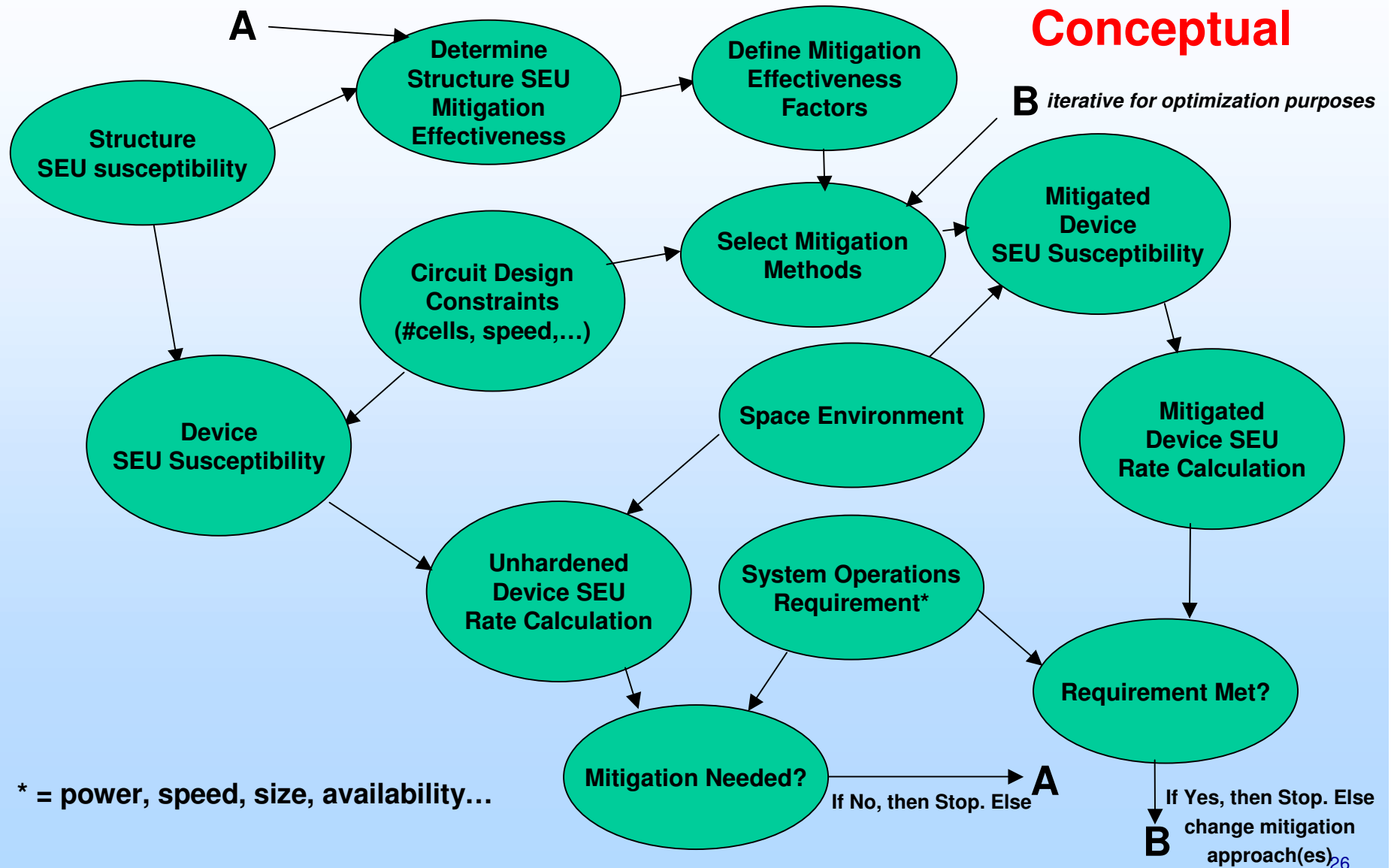# System Validation Considerations: Aeroflex vs. Xilinx

- **Aeroflex:**
  - Failure Rate Prediction is ongoing research at this point
  - Recovery time will generally be shorter due to the anti-fuse structure of configuration (I.e. no configuration download)
  - Mitigation is built into the silicon (DICE Cells) and therefore simplifies System Validation after mitigation
  - Due to the increase in the number of devices, System Validation will increase slightly

- **Xilinx:**
  - Failure Rate Prediction is ongoing research at this point
  - Recovery time will generally be longer due to the necessity of configuration download
  - Mitigation is inserted after synthesis. System Validation can be complicated for XTMR (it should be proven that every DFF has the proper mitigation and that no functionality has been disrupted during XTMR insertion).
  - Extra mitigation circuitry must also be validated: I.e. the Scrubbing logic (includes extra FPGA as the scrubber, board level mitigation, and Flash Memory Mitigation).

Optimizing A Solution – Is it Realizable?

Conceptual

A → **Determine Structure SEU Mitigation Effectiveness** → **Define Mitigation Effectiveness Factors**

B *iterative for optimization purposes*

Structure SEU susceptibility

Circuit Design Constraints (#cells, speed,…) → **Select Mitigation Methods** → **Mitigated Device SEU Susceptibility**

Device SEU Susceptibility

Space Environment

Mitigated Device SEU Rate Calculation

Unhardened Device SEU Rate Calculation

System Operations Requirement*

Requirement Met?

Mitigation Needed? → **A** If No, then Stop. Else

If Yes, then Stop. Else change mitigation approach(es)

B

* = power, speed, size, availability…

Summary

- **This presentation has shown a simplistic view of some of the trade spaces involved with FPGA selection and use for space applications**
- **Frankly, good designers can almost always come up with an approach that can work**
  - **However, optimizing the solution space for specific parameters such as weight or power or system operability must be thoroughly considered**